Process-Induced Deformations and Stacking Faults in 4H-SiC

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ABSTRACT

We used Film Stress Measurement (FSM), Transmission Electron Microscopy (TEM), and High-Resolution X-ray Diffraction (HRXRD) techniques to obtain further knowledge with respect to the deformation, warpage, and stacking faults (SF's) that are induced in n-type 4H-SiC wafers and epilayers when subjected to mechanical polishing and high temperature (1150 ^{o}C) processing.

INTRODUCTION

Silicon carbide semiconductor has been attracting growing attention over the past three decades, particularly due to its potential applications in high power and high temperature electronics and sensors. This is as a result of its superior electrical and high temperature properties over conventional semiconductor materials. A variety of electronic and sensing devices fabricated in single crystal SiC, particularly in the hexagonal 4H- and 6H- polytypes, have been demonstrated and a few are commercially available and deployed in the field. One of the major benefits of SiC electronics is its potential application as a high voltage PiN rectifier diode, which has been demonstrated to block voltage as high as 10 kV [1]. However, the presence of several kinds of structural defects in the crystal has, in general, been largely responsible for the performance of these devices at below theoretical levels. The presence of Stacking Faults (SFs), in particular, is recognized to be the primary defect that degrades the electrical performance of PiN diodes over time [2]. Their deleterious effects are more severe given that they exist (or are generated) in the active region of the device.

Two well-established conditions under which these SFs form are during high temperature processing of n-type 4H-SiC and during the forward bias operation of 4H-SiC-based PiN diodes. Under the former condition, SFs that lead to the formation of 3C-like bands in n-type 4H-SiC epilayer doped 1.7 x 10^{19} cm^{-3} were discovered after routine thermal oxidation or argon annealing at 1150°C [3]. In the latter case, the SFs were observed to form and enlarge driven by electron-hole recombination during PiN diode forward bias operation [2]. Generally, because the SF mimics the 3C-SiC (E_g=2.4 eV) crystal structure, its presence as an inclusion in 4H-SiC (E_g=3.2 eV) makes it electronically behave as a one-dimensional quantum well (QW) with carrier transport predominantly confined along the basal plane. Under such condition, the overall electronic properties of the crystal structure are fundamentally altered to the extent that the primary desired diode current conduction perpendicular to the basal plane is practically blocked, thereby severely degrading the bipolar device's on-state performance. The total energy calculations by Lindefelt *et al*. and Miao *et al*. of a 4H-SiC crystal with intrinsic SF inclusion found that a narrow band is split off from the bottom of the conduction band and extends about 0.2 eV into the bandgap of 4H-SiC

[4, 5]. Liu *et al.* had proposed the formation mechanism of the thermal-induced SFs to be a spontaneous process in which thermally generated carriers are transported and trapped in the QW thus lowering the energy of the crystal [6]. Subsequently, Kuhr *et al*. calculated a threshold nitrogen doping concentration of 3 x 10^{19} cm^{-3} to be the lowest limit for such a process, below which thermally generated SFs are not expected to form [7].

This paper focuses only on the thermally generated SFs. It will discuss conditions under which these SFs are formed and also provide further insight with regard to the effects of chemical mechanical polishing (CMP) of the Carbon-face (C-face) of 4H-SiC wafers on the overall structure of the crystal. A comparative analysis of the residual stresses in the epilayers that are grown on the Si-face of wafers with both polished and unpolished C-face backsides will also be presented. Internal stresses in semiconductor substrate materials have previously been recognized to adversely impact the yield and reliability of electronic devices [8]. Numerical simulations have been widely used to understand the stress levels in SiC boules, but little is known about the residual stress in SiC wafer epilayers. This paper presents experimental results of how wafer backside CMP and thermal treatment can combine to induce structural changes in 4H-SiC wafers and epilayers.

EXPERIMENTS

Two sets of experiments were performed. Experiment-1 investigated the range of doping that makes an epilayer susceptible to SFs when thermally processed at high temperature up to 1150 ^{o}C. Experiment-2 was to quantify the structural changes induced in 4H-SiC wafers after backside CMP while determining the effects of such process on epilayers grown on the wafer. In the first experiment, three each of n- and p-type 4H-SiC wafers with *unpolished* C-face backsides had 2 μm n-type epilayers homoepitaxially grown on the polished Si-face. The epilayer doping levels ranged from 5.2 x 10^{17} to 2 x 10^{19} cm^{-3}. While details of the process steps and description of the Film Stress Measurement (FSM) and High Resolution Transmission Electron Microscopy (HRTEM) analyses can be found in [9, 10], an outline of the FSM process is as follows. The tool employs an optical measurement technique whereby a diode laser beam scans across the diameter of the wafer that is placed on the tips of metal tripods. The tripods extend out 2 mm above the plane of a heater plate; this tripod arrangement provides very small contact areas with the wafer. The reflected beam undergoes a secondary reflection by a mirror and is detected by a precision position photo-detector. By scanning the diameter of a wafer while the reflected beam is continuously detected, the wafer bow along the entire wafer diameter is obtained, thereby allowing for the direct calculation of the spatially distributed radius of curvature of the wafer. The initial and the final curvature, R_o, and R_{o2}, were measure before heating to 500 ^{o}C and after cooling down to room temperature, respectively. From the radius of curvature after epilayer growth, R_{epi}, the biaxial stress in the epilayer was calculated by using Stoney's equation [11].

In Experiment-2, FSM and High Resolution X-ray Diffraction (HRXRD) curvature measurements were performed on three n-type Si-face polished (8° off axis) 4H-SiC wafers [(N_d = 0.636, 1.1, and 2.13) x 10^{19} cm^{-3}] before and after CMP of the C-face and after 2 μm n-type homoepitaxial growth on the Si-face having nitrogen concentration of 1x10^{19} cm^{-3}. The measurement of the wafer curvature by HRXRD method before and after epilayer growth also made it possible to apply Stoney's equation to quantify the residual stress in the epilayer after growth. For the HRXRD analysis, the equipment was a Bede D1 system 2-bounce Si 220 asymmetric beam conditioner with a Max Flux mirror, operated at 40KV, 30mA, and with a 0.1 mm slit before the sample, a 1 mm slit after the sample (before the detector). For triple-axis

diffraction, another 2-bounce Si 220 asymmetric monochromator was used as the analyzer. Sample orientation was Si face, 8° off-cut toward the right $\langle 11\bar{2}0 \rangle$ direction, 0008 reflection, incidence angle, $\theta_B - 8° = 29.695°$, and exit angle $\theta_B + 8° = 45.695°$. For the double axis rocking curve, the wafers were linearly scanned along the $\langle 11\bar{2}0 \rangle$ direction from one wafer edge to the other to obtain position-dependent microstructure information on crystal quality.

RESULTS AND ANALYSES

Experiment 1-FSM and TEM Analysis
The radii of curvature for the wafers before and after thermal treatment to 500 °C, and after epilayer growth are given in Table 1. After epitaxial growth, the residual stress was calculated and is also presented in Table 1. No strong correlation was found between the epilayer residual stress and doping level. Previously published x-ray diffraction measurement of doping induced lattice mismatch also indicated that only a negligible strain was induced in the epilayer [12]. Following thermal processing at 1150 °C in nitrogen and HRTEM analysis, SFs were discovered on the basal plane, along the $\langle 11\bar{2}0 \rangle$ direction in all the samples, including the sample with epilayer doping level of 5 x 10^{17} cm^{-3}. This is shown in Figures 1a-c. It is important to note that SFs are observed in all the samples even for the lowest doping level that is two orders of magnitude below the proposed threshold (3 x 10^{19} cm^{-3}) required for the onset of the generation of SFs in annealed

Table 1: Changes in wafer radius of curvature of un-polished backside 4H-SiC wafers before (R_o) and cooled down from 500 °C (R_{o2}), after epilayer growth (R_{epi}), and the corresponding residual stress.

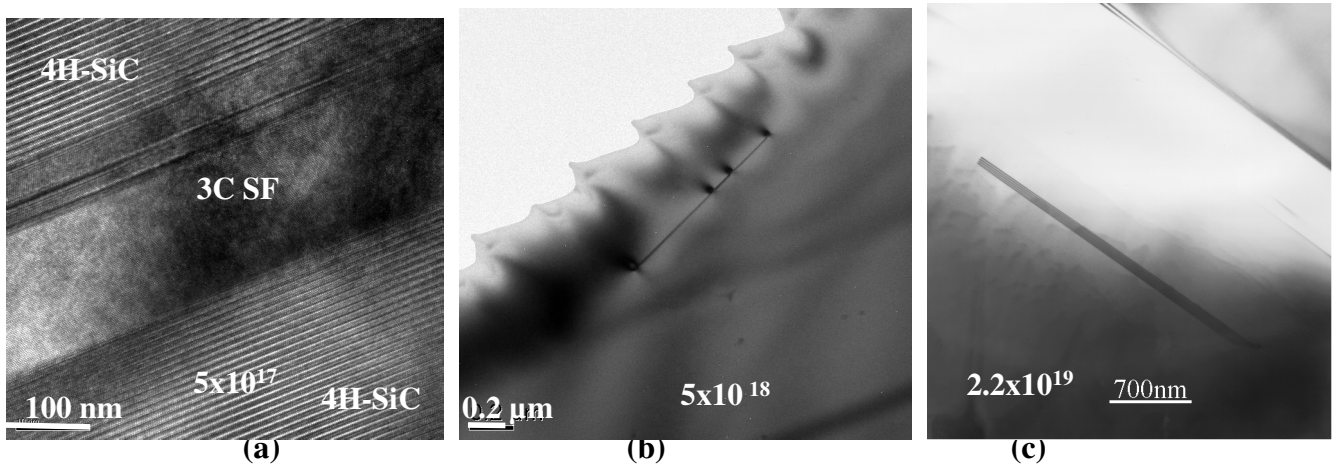| Sample	Substrate ρ (Ω-cm)	R_o (m)	R_{02} (m)	Epi Doping (cm^{-3})	R_{epi} (m)	Epi Stress (MPa)
P1	9.57	10.47	18.63	2 x 10^{19}	35.83	-199.6
P2	4.72	8.53	12.84	3.9 x 10^{18}	19.7	-211.2
P3	4.42	10.87	20.42	5.2 x 10^{17}	41.31	-190.0
N1	0.01	13.2	15.6	2 x 10^{19}	32.5	-251
N2	0.011	38.6	76.7	5 x 10^{18}	-24.4	-406.1
N3	0.011	18.6	23.6	5 x 10^{17}	-122.9	-376.1
4* on-axis	0.007	6.9	6.4	N/A	N/A	N/A

(a) (b) (c)

Figure 1: Cross sectional TEM images of 8° off-axis n-type 4H-SiC epilayers with doping a) 5 x 10^{17} cm^{-3}, b) 5x10^{18} cm^{-3}, and c) 2.2x10^{19} cm^{-3}, 2 μm thick annealed for 30 minutes at 1150 °C in a nitrogen ambient. In all cases, the backsides C-face of the wafers were unpolished.

*The on-axis wafer was unaffected by the thermal process.

epilayers on the basis of QW action [7]. The Fermi energy levels corresponding to these lower doping levels are tenths of eV below the (E_c-0.2) eV level of the SF split off band at room temperature. Therefore, the density of thermally generated carriers is not sufficient to raise the Fermi level to the E_c-0.2 eV split off band level. This makes the carrier interaction with the SF QW less likely. Because SFs cannot be thermally generated via QW action at this low doping level, this result strongly suggests the existence of another driving force for SF generation. From Table 1, the product of the epilayer residual bi-axial stress (σ) and the Schmid factor ($\cos\zeta\cos\phi$, where ζ and ϕ represent the angle from the slip plane normal to the loading axis and angle of the slip direction to the loading axis) resolves the shear stress, τ, on to the basal plane and was estimated to be between 20 and 70 MPa. The potential for plastic deformation increases under such shear stress level on the basal plane, as evidenced by the change in the wafer curvature (see Table 1). Also, the resolved shear stress is more than required to overcome the Peierls energy barrier of the partial dislocation from where it is suspected the SF nucleates, thereby allowing for its expansion to create the SFs.

Experiment 2-FSM and HRXRD Analysis

In all three cases, the virgin un-polished wafers were generally curved upward on the Si-face, except for one wafer with a bi-modal shape. However, after heating to 500 ^{o}C and polishing the backside C-face, the curvatures of all the wafers changed polarity to the C-face, as seen in the representative plots of Fig. 2. Subsequent growth of a 2 μm n-type, $1x10^{19}$ cm^{-3} epilayer and heating to 1150 ^{o}C did not reveal any further significant change in the curvature or polarity. This result was in sharp contrast with the result obtained in the first experiment in which the epilayer grown on the on Si-face with un-polished c-face backside led to a significant change in the wafer curvature (see Table 1).
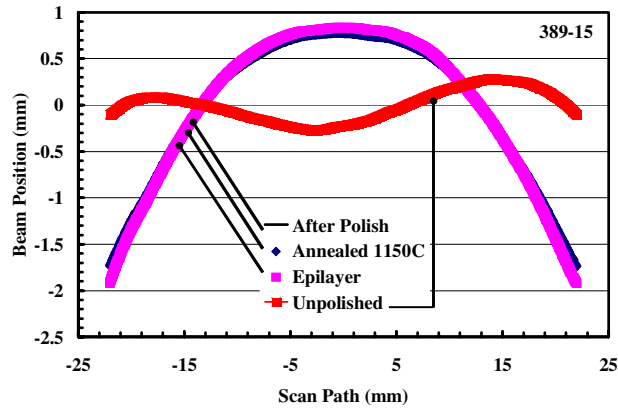

Figure 2: Representative FSM plots of 4H-SiC wafer curvature before and after polishing, after a 2 μm homoepitaxial growth, and annealing.

Table 2: FSM and XRD measured changes in radius of curvature at different process steps. The large difference in sample 382-8 was due to the bi-modal curvatures associated with warpage.

Method	Sample	$R_{(pre-polish)}$ (m)	$R_{(post polish)}$ (m)	$R_{(post epi)}$ (m)	Res. Stress (MPa)
FSM	382-8	57.75	111.54	64.73	21.3
XRD		17.73	-35.21	-38.91	8.88
FSM	389-15	14.37	-13.55	-13.34	-3.2
XRD		20.83	-28.90	-26.88	-8.55
FSM	835-2	19.87	-18.17	-19.12	8.99
XRD		22.22	20.16	19.57	4.03

Stress analysis was also performed with HRXRD method. During the linear scanning of the wafer, the peak position kept shifting to the high-angle side when the beam was scanned across the wafer. The peak shift, $\delta\theta$, increased almost linearly with position. Since the lattice constant of the wafer is homogeneous across the wafer, the linearly increasing $\delta\theta$ with position indicated that the (0001) lattice planes are curved. In all three cases (see Fig. 3), $\delta\theta$ increases almost linearly with

position. Figure 3 shows the representative full width at half maximum (FWHM) values of the double-axis rocking curves (DRCs) measured from different regions of one of the wafers at various stages of the experiment. The peak positions are also shown for calculating the curvature. This result was consistently reproduced in the other wafers. The position-dependent FWHM values obtained before C-face polishing of a representative wafer are plotted in Fig. 3a. The curvature determined from the slope of the fitted line was 4.8×10^{-2} m^{-1}. Figure 3b shows the data from the same wafer after the CMP of the backside C-face. The FWHM values of most areas on the Si-face are around 30 arcsecs ("). The lowest FWHM value is 26.1", which is close to the theoretical value corresponding to a perfect crystal. Meanwhile, for almost all the areas the local FWHM values after CMP of the back C-face are very close to the values measured before CMP. This indicates that the CMP of the backside C-face has little influence on the local crystalline quality of the Si face. However, as indicated by comparing Fig. 3a to 3b, CMP changes the curvature polarity of the entire wafer. In other words, the curvature center changes from the Si face side before CMP to the C-face after backside CMP. Except for sample 382-8 (see Table 2), this is in good agreement with the FSM measurement, implying that the CMP process introduced macroscopic strain (bending) to the wafer. Compared to the post-polish measurements, very little additional change in the radius of curvature occurred after the epitaxial growth as seen in Fig. 3c.
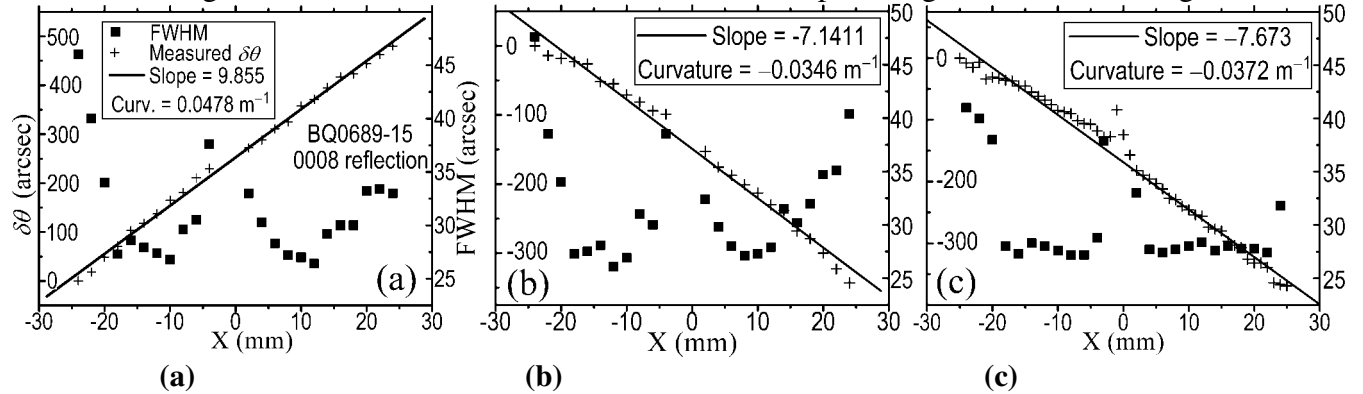

Figure 3: Position-dependent FWHM values (black squares, associated with the right axis) and Bragg peak shifts for the three wafers, a) before backside CMP, b) after CMP, and c) after epilayer growth.

From the curvature measurement obtained by HRXRD, the residual bi-axial stress in the epilayer was also calculated with Stoney's equation and presented in Table 2. A comparison of the residual stress obtained by HRXRD with the FSM technique shows that, within the limits of experimental error, the measured curvatures were in relatively good agreement, except for sample 382-8 with bi-polar curvature. In general, the residual stresses using both measurement techniques were compressive in nature. The absolute values of the stress are also in relatively good agreement, with resolved shear stresses on the basal plane along the $\langle 11\bar{2}0 \rangle$ direction of between 1 and 4
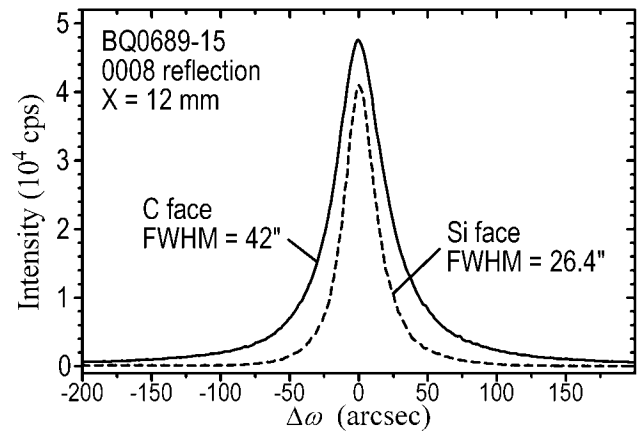

Figure 4: Comparison of the DRC measured form the same region but on different faces.

MPa. It is worth noting that these values are much lower than the previous values obtained in Experiment-1 for epilayers grown with the backside C-face unpolished.

For the XRD measurements conducted on the unpolished C-face, the FWHM was consistently larger relative to that on the polished Si-face. A representative example is shown in Fig. 4 in which the FWHM on the C-face at point X=12 mm is 42", which is much larger than that at the corresponding area of the polished Si face, 26.4". This means that the unpolished C-face backside surface is significantly strained, in both lattice constant and lattice tilt. This is very significant, as it indicates that the standard SiC wafer before backside CMP and epitaxy is already macroscopically strained.

CONCLUSION

The TEM findings clearly indicated that SFs can be generated by high temperature (1150 ^{o}C) processing of epilayers with n-type doping concentration as low as 5×10^{17} cm^{-3}. At these doping levels, the Fermi energy lies well below the SF split off energy band that corresponds to the 3C-SiC QW. Thus the density of thermally generated carriers that are transported and trapped in the SF QW is not sufficient to lower the crystal energy by causing the SFs to form. This experimental result cannot be explained with the model presented in [7]. As the doping level decreased, the density of SFs also decreased. We have also used FSM and HRXRD to measure changes in wafer curvature at wafer processing steps of wafer backside polishing, thermal treatment, and epilayer deposition. The results showed consistent switch in wafer curvature polarity after backside C-face polishing. Our results also showed that significant residual stress was removed from the epilayer grown on Si-face wafers when the C-face backside of the wafer was polished prior to epilayer deposition. We are, however, yet to determine if the polish-induced reduction of the residual shear stress would lead to a corresponding decrease in the density of SFs in these epilayers.

ACKNOWLEDGEMENT

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